What is claimed is:

1. A circuit for detecting an abnormal operation of memory comprising: a delay circuit for delaying an output data of the memory for a predetermined period of time and for outputting this data as a delay data; and

a comparison circuit for outputting an incoincidence signal in case that the output data of the memory and the delay data are not coincident with each other after compared.

2. A circuit for detecting an abnormal operation of memory according to claim 1 wherein an abnormal operation with regard to an access speed of memory is detected.

3. A circuit for detecting an abnormal operation of memory according to claim 1 further comprising a circuit for holding address information in case of an incoincidence in response to the incoincidence signal.

4. A circuit for detecting an abnormal operation of memory according to claim 1 further comprising a circuit for sounding an alarm in outputting the incoincidence signal.

5. A circuit for detecting an abnormal operation of memory according to claim 1 further comprising a circuit for executing an interruption in outputting the incoincidence signal.

6. A circuit for detecting an abnormal operation of memory according to claim 1 wherein a delay time of the output data of the memory can be adjusted in the delay circuit.

7. A circuit for detecting an abnormal operation of memory according to claim 1 wherein the memory is a flash memory.

8. An integrated circuit comprising a circuit for detecting an abnormal operation of memory according to claim 1.

9. A method for detecting an abnormal operation of memory comprising the steps of: delaying an output data of memory for a predetermined period of time and of outputting this data as a delay data; and

outputting an incoincidence signal in case that the output data of the memory and the delay data are not coincident with each other after compared.

10. A method for detecting an abnormal operation of memory according to claim 9 wherein an abnormal operation with regard to an access speed of memory is detected.

11. A method for detecting an abnormal operation of memory according to claim 9 further comprising the step of holding address information in case of an incoincidence in response to the incoincidence signal.

12. A method for detecting an abnormal operation of memory according to claim 9 further comprising the step of sounding an alarm in outputting the incoincidence signal.

13. A method for detecting an abnormal operation of memory according to claim 9 further comprising the step of executing an interruption on a CPU in outputting the incoincidence signal.

14. A method for detecting an abnormal operation of memory according to claim 9 further comprising the step of rewriting in a memory in outputting the incoincidence signal.

15. A method for detecting an abnormal operation of memory according to claim 9 wherein a delay time of the output data of the memory can be adjusted in the delaying step.

16. A method for detecting an abnormal operation of memory according to claim 9 wherein the memory is a flash memory.